High Efficiency 500kHz 2A Synchronous Step Down Converter

1 Features

- 4.5V to 36V Input Voltage Range
- 0.6V Reference Voltage
- 2A Output Current
- Low R_{DS_ON} 150/78mΩ (High/Low-Side)
- 500kHz Switching Frequency
- Internal 1.3ms Soft-Start Time
- Internal Compensation Function
- Over Current Protection
- Hiccup Short Circuit Protection
- Over Temperature Protection
- RoHS Compliant and Halogen-Free

2 Applications

- White goods
- Audio devices
- Set Top Box, Digital TV

3 Description

The GD30DC1354 is a high efficiency synchronous DC/DC step-down converter. The device operates from an input voltage from 4.5V up to 36V.The main switch and synchronous switch are integrated in the device with very low R_{DS_ON} and capable of delivering up to 2A current.

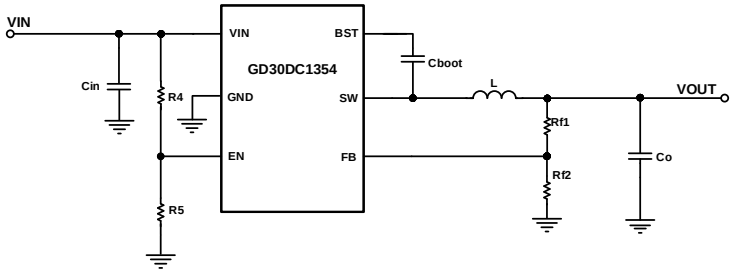
The switching frequency is set at 500kHz to minimize output voltage ripple. The GD30DC1354 fault protection includes over current protection, short circuit protection, under voltage lockout protection and thermal shutdown. The Internal soft-start function prevents inrush current at turn-on. The GD30DC1354 is offered in SOT23-6 packages.

Device Information[1]

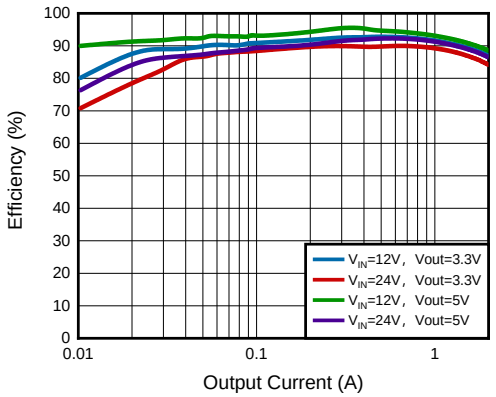
PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1354	SOT23-6	1.60mm x 2.90mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



Efficiency vs Output Current



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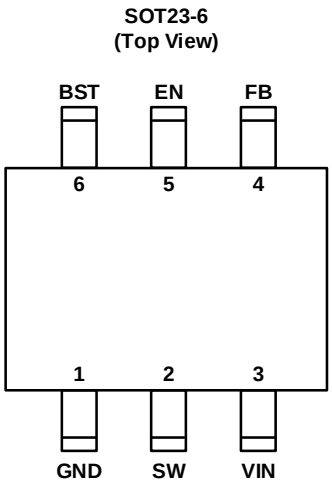
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	SOT23-6		
GND	1	G	**Power ground.**
SW	2	O	**Switch output**. Switch pin connected to the internal MOSFET switches and inductor terminal.
VIN	3	P	**Power supply voltage**. Operates from a 4.5V to 36V input rail. A decoupling capacitor is required to decouple the input.
FB	4	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider.
EN	5	I	**Enable**. Floating to enable or pull-down to disable. Adjust the input under-voltage lockout with two resistors.
BST	6	O	**Bootstrap**. Connect a BST capacitor between SW and BST to form a floating supply across the high-side switch driver.

1. I = Input, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Input voltage	−0.3	38	V
V_{SW}	Switching node voltage (SW)	−0.3	V_{IN} + 0.3	V
V_{IO}	I/O pin voltage (EN, FB)	−0.3	6	V
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−65	150	°C
P_{max}	SOT23-6 Maximum power dissipation @ T_A=+25°C		0.4	W

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	4.5		36	V
V_{OUT}	Output voltage range	0.6		V_{IN} * D_{MAX}	V
I_{OUT}	Output current			2	A
T_J	Operating junction temperature	-40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	SOT23-6	89.2	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	SOT23-6	14.7	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	SOT23-6	39.5	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	SOT23-6	14.7	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	SOT23-6	1.2	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = V_{EN} = 5V, T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$V_{IN(OVP)}$	Input overvoltage protection		4.5		36	V
I_Q	Quiescent current	No switching		300		μA
I_{SHDN}	Shutdown current	EN = 0V		2		μA
V_{UVLO}	Under voltage lockout	V_{IN} Rising V_{IN} falling		4.2 4.05		V
V_{UVLO_HYS}	Under voltage lockout hysteresis			150		mV
ENABLE						
V_{EN_RISE}	Rising enable threshold	2.5V ≤ V_{IN} ≤ 5.5V		1.27		V
V_{EN_FALL}	Falling enable threshold	2.5V ≤ V_{IN} ≤ 5.5V		1.23		V
VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{IN} = 2.5 to 5.5V	0.585	0.6	0.615	V
I_{FB}	Feedback leakage current	V_{FB} = V_{IN}		2		nA
INTEGRATED POWER MOSFETS						
$R_{DS(on)}$	High-side FET on resistance			150		mΩ
	Low-side FET on resistance			78		mΩ
SWITCHING REGULATOR						
F_{SW}	Switching frequency	I_{OUT} = 300mA		500		kHz
T_{MIN}	Minimum on time1			100		nS
CURRENT LIMIT						
I_{LIM}	High-side current limit[1]			4.5		A
I_{LIM}	Low-side current limit[1]			4.0		A
THERMAL SHUTDOWM						
T_{TSD}	Thermal shutdown temperature[1]			160		°C
T_{HYS}	Thermal shutdown hysteresis[1]			10		°C

1. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

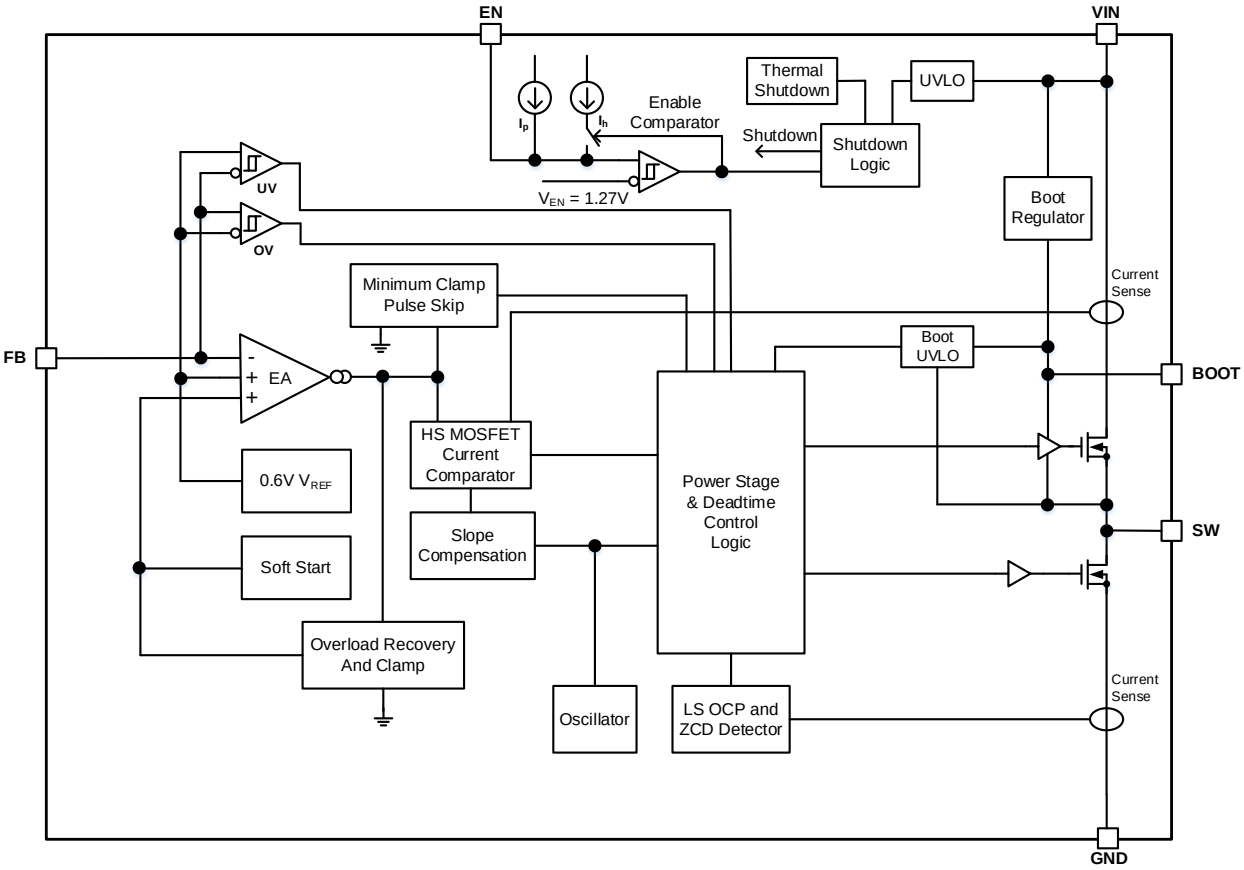


Figure 1. GD30DC1354 Functional Block Diagram

6.2 Operation

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load, line response, protection of the internal main switch and synchronous rectifier. The GD30DC1354 switches at a constant frequency and regulates the output voltage. During each cycle, the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until next cycle starts.

6.2.1 Pulse Frequency Modulation

The device automatically enters Pulse Frequency Modulation(PFM) to improve efficiency at light load when the inductor current becomes discontinuous. In discontinuous conduction mode(DCM), the low-side switch is turned

off when the inductor current drops to approximately 0A. When feedback voltage(V_{FB}) drops below the reference voltage, the high-side FET is turn on. In PFM mode, the switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions. PFM mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency. Also, small increase in output voltage occurs at light loads.

6.2.2 Soft Startup

The device employs internal soft start function to reduce input inrush current and creates a smooths output voltage rise slope during start up. The internal soft start time is set to 1.3ms.

6.2.3 Error Amplifier

The device has a trans-conductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower of the internal soft-start voltage or the internal 0.6V voltage reference. The transconductance of the error amplifier is 35μA/V typically. The frequency compensation components are placed internal between the output of the error amplifier and ground.

6.2.4 Under Voltage Lockout

To avoid mis-operation of the device at an insufficient supply voltage, implement under voltage locking to shutdown the device when the voltage is below the V_{HYS} hysteresis of the V_{UVLO}.

6.2.5 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

The over-current protection(OCP) of high-side MOSFET is implemented in this device, which uses the COMP voltage output by the internal error amplifier to control the turn-off of high-side MOSFET on a cycle-by-cycle. Each cycle, the current reference generated by the internal COMP voltage is compared with the inductor current. If the peak current value exceeds the set current limit threshold, the high-side MOSFET is turns off.

The device not only implements the high-side overcurrent protection, but also provides over source current protection and over sink current protection for low-side MOSFET. When the low-side MOSFET is turned on, the internal circuit continuously monitored the inductor current. In normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the sourcing current limit set internally. When the inductor valley current is higher than the source current limit, the high-side MOSFET is turned off, and the low-side MOSFET kept on for the next cycle. The high-side MOSFET turned on again only when the inductor valley current is below the source current limit at the start of a cycle as shown in Figure 2.

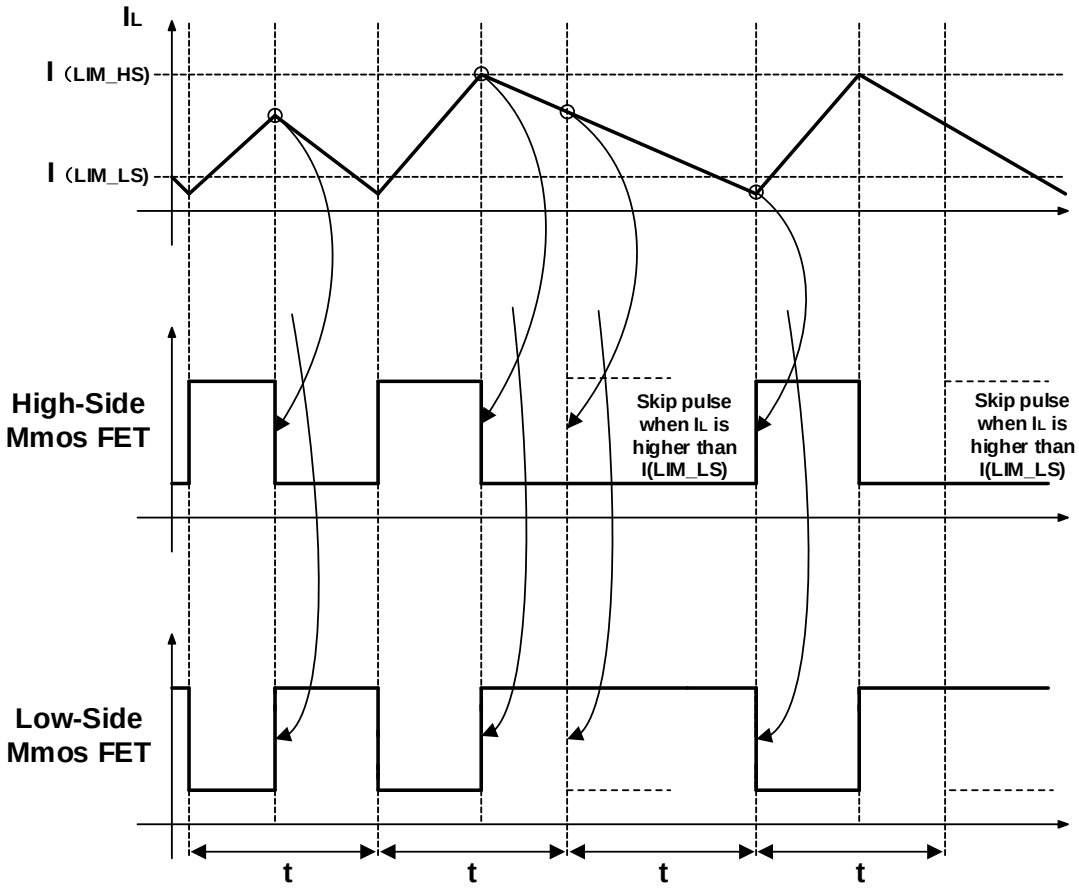


Figure 2. Overcurrent Protection for Both MOSFETs

6.2.6 Output Over-Voltage Protection

The device provides an output overvoltage protection(OVP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVP circuit minimizes overshoot by comparing the FB pin voltage to the OVP threshold. When the FB pin voltage is higher than 106% × V_{REF}, the high-side MOSFET will be forced off. When the FB pin voltage falls below 104% × V_{REF}, the high-side MOSFET will be enabled again.

6.2.7 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C(typical), both the high-side and low-side FETs are turned off. Once the device temperature falls below the threshold with hysteresis 10°C (typical), the device returns to normal operation automatically.

6.3 Device Mode Description

6.3.1 Device Enable

The EN pin provides electrical control to turn on/off the regulator. When VEN exceeds the threshold voltage 1.27V, the regulator starts operation. If VEN is below the shutdown threshold voltage 1.23V, the regulator shut down and enters to low quiescent current about 2μA.

Additionally, the EN pin, due to the pull-up current source inside the device, allows the user to enable the device when the EN pin floats. If the application needs to control the EN pin, an external MOSFET or BJT can be added to implement digital control from the EN pin to the ground.

To prevent the malfunction of too low supply voltage, the device implements an internal UVLO circuit on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold, and the internal VIN-UVLO hysteresis threshold is 150mV.*VIN UVLO Setting.*

If an application requires either a higher UVLO threshold on the VIN pin, then EN pin can be configured as shown in Figure 3.

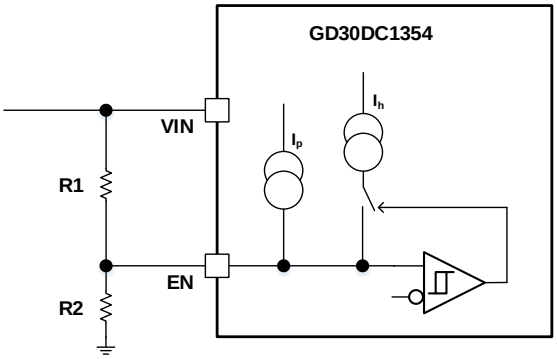


Figure 3. VIN UVLO Setting

Without external components, the internal pull-up current Ip sets the EN pin default status to Enable. The pull-up current is also used to control the voltage hysteresis for the UVLO function, which increases I_h when the EN pin voltage exceeds the enable threshold.

The UVLO thresholds can be calculated using Equation(1) and Equation(2).

$$R1 = \frac{V_{START} \times (\frac{V_{EN\_FALLING}}{V_{EN\_RISING}}) - V_{STOP}}{I_p \times (1 - \frac{V_{EN\_FALLING}}{V_{EN\_RISING}}) + I_h} \quad (1)$$

$$R2 = \frac{R1 \times V_{EN\_FALLING}}{V_{STOP} - V_{EN\_FALLING} + R1 \times (I_p + I_h)} \quad (2)$$

Where I_h = 2.1μA, I_p = 0.7μA, V_{EN_RISING} = 1.27V, $V_{EN\_FALLING}$ = 1.23V

7 Application Information

The GD30DC1354 device is typically used as a step down converter, which convert an input voltage from 8V to 36V to fixed output voltage 5V.

7.1 Typical Application Circuit

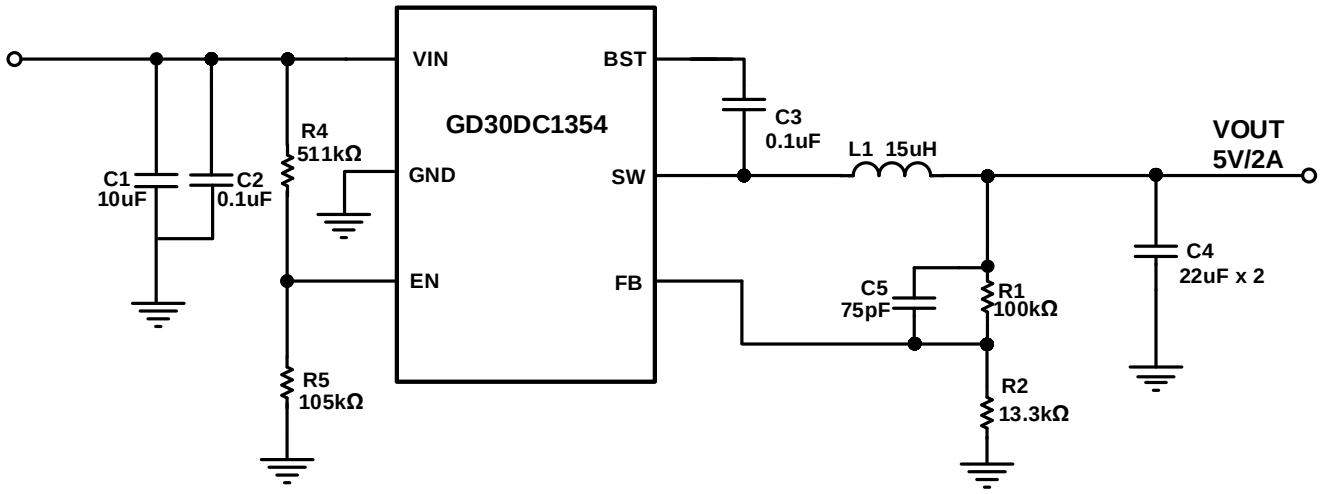


Figure 4. 5V, 2A Reference Design

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	8V to 36V
Output Voltage	5V
Maximum Output Current	2A

Table 2 lists the components used for the example.

Table 2. Design Example Component[1,2]

COMPONENT	DESCRIPTION
C1,C2	10uF,0.1 uF, Ceramic Capacitor, 10V, X7R, size 0603
L1	15uH, Power Inductor
R1,R2	Divider resistor, 1%, size 0603
C5*	Optional, 10pF if it is needed

1. The components used in these design cases do not belong to GD products, GD does not warrant its accuracy or completeness. GD's customers need to test and verify whether the selected components meet their intended use to ensure stable system operation.*Design Parameters*
2. Refer to *Detailed Design Description* section for guidance on component selection and calculation equations.

7.3 Detailed Design Description

7.3.1 Output Voltage Setting

An external resistor divider is used to set output voltage according to Equation(3). By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage reference at the FB pin is 0.6V.

$$V_{OUT} = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

The feedback circuit is shown in Figure 5.

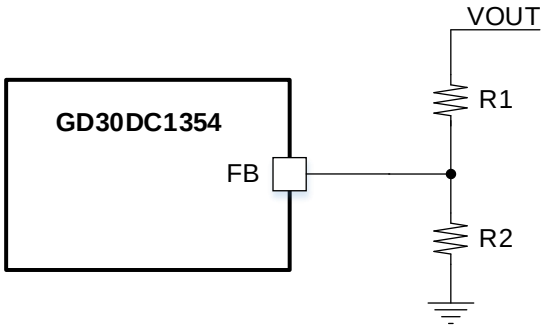


Figure 5. Feedback resistor divider

Table 3 lists the recommended parameters values for common output voltages.

Table 3. Component selection for common output voltages

VOUT(V)	R1(KΩ)	R2(KΩ)	L(uH)
1.2	20	20	2.2
3.3	100	22.1	10
5	100	13.3	15
12	100	5.23	22

7.3.2 Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, inductors with larger inductance and low DCR values provide much more output and high conversion efficiency, and smaller inductance values can give batter load transient response.

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 40% of the IC rated current. And the peak inductor current can be calculated by Equation(4) and Equation(5). Ensure that the peak inductor current is below the maximum switch current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(MAX)} \quad (4)$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \quad (5)$$

The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value according to Equation(6). Once an inductor value is chosen, the peak inductor current is determined by Equation(5). Attention that the inductor should not saturate under the inductor peak current.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (6)$$

7.3.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The input capacitance value determines the input voltage ripple of the converter. For most applications, a 10μF capacitor is sufficient.

The peak-to-peak voltage ripple on input capacitor can be estimated with Equation(7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For best performance, ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To compensate the derating of the ceramic capacitors, the voltage rating of capacitor should be twice of the maximum input voltage. The input capacitor also requires an adequate ripple current rating since it absorbs the input switching current.

The input ripple current can be estimated with Equation(8):

$$I_{CIN} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (8)$$

Where D is the duty cycle of converter. The worst-case condition occurs at $V_{IN} = 2V_{OUT}$. At this point, the input ripple current of input capacitance is equal to half of output current. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

7.3.4 Output Capacitor Selection

The output capacitor stabilizes the DC output voltage, it directly affects the steady state, output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient.

The output voltage ripple can be estimated with Equation(9):

$$\Delta V_{OUT} = \Delta I_L \times \left(C_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (9)$$

The output capacitor ripple is essentially composed of two part. One part is caused by the inductor ripple current flowing through the ESR of output capacitors, another part is caused by the inductor ripple current charging and discharging output capacitors. For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. And when using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

The output capacitance must be large enough to supply the current when a large load step occurs. But if the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft start time. Two 22uF Ceramic capacitors are recommended in this application.

7.4 Power Dissipation

For DC/DC, these is still some power deposited on the chip and converted into heat, in spite of switch mode power supplies have considerably higher efficiency when compared to linear regulators. The device power dissipation includes conduction loss, switching loss, gate charge loss and quiescent current losses. The maximum allowable continuous power dissipation at any ambient temperature is calculated by Equation(10):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (10)$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance. Once exceeding the maximum allowable power, The device enters thermal shutdown to avoid permanent damage.

7.5 Typical Application Curves

V_{IN} = 12V, V_{OUT} = 5V, L = 15uH, T_A = 25°C, unless otherwise noted.

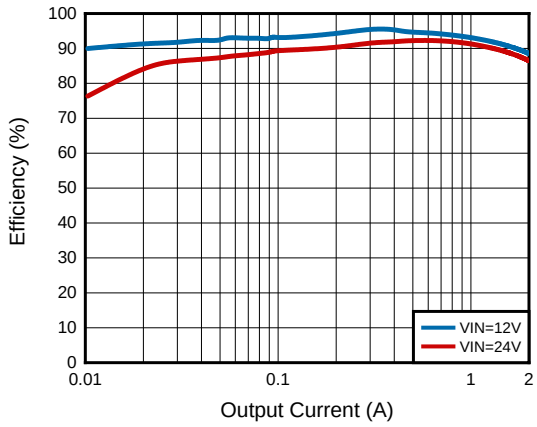


Figure 6. 5V Output Efficiency

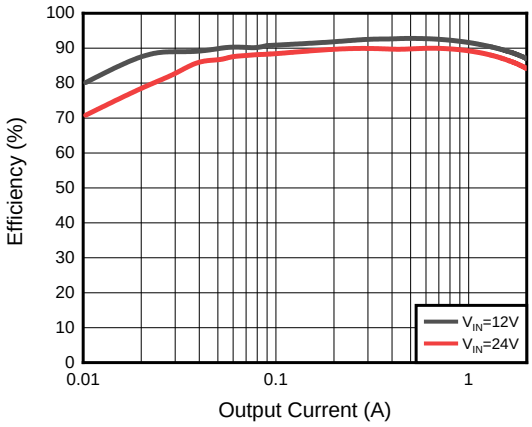


Figure 7. 3.3V Output Efficiency

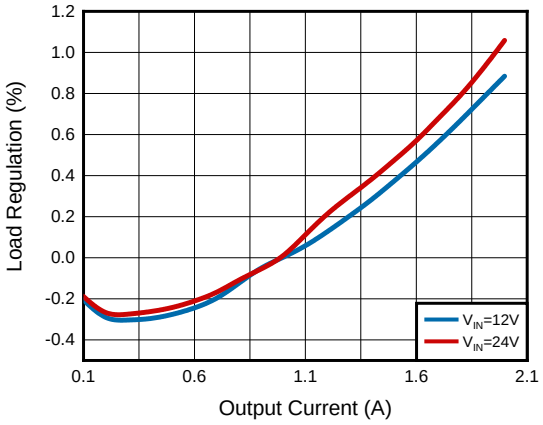


Figure 8. Load Regulation

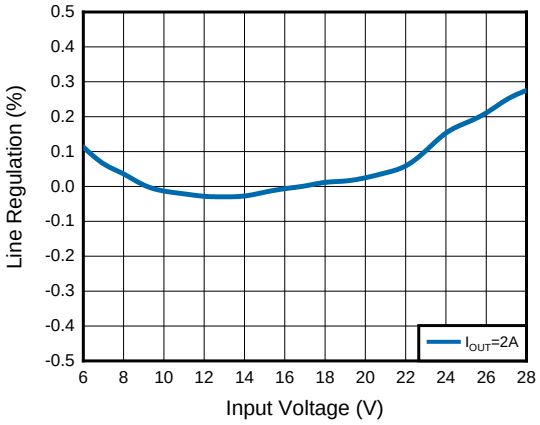


Figure 9. Line Regulation

Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 5V, L = 15uH, T_A = 25°C, unless otherwise noted.

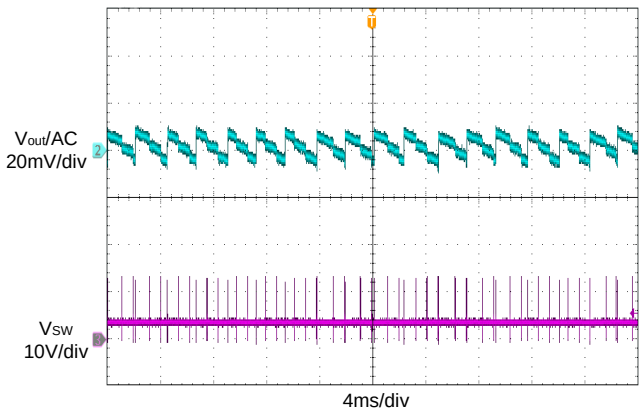


Figure 10. Output Voltage Ripple (I_{OUT}=0A)

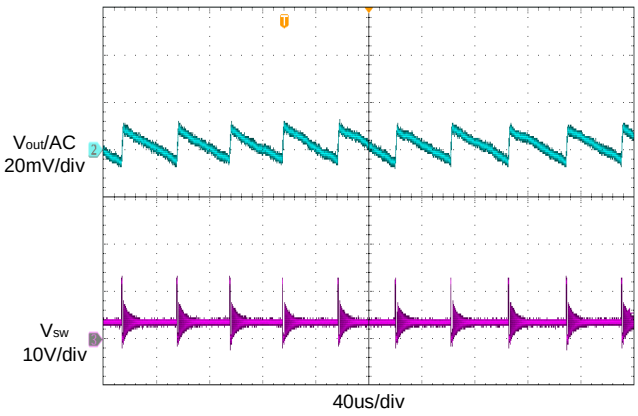


Figure 11. Output Voltage Ripple (I_{OUT}=10mA)

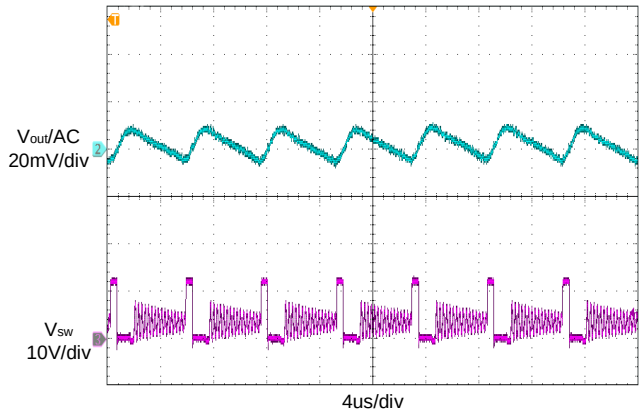


Figure 12. Output Voltage Ripple(I_{OUT}=100mA)

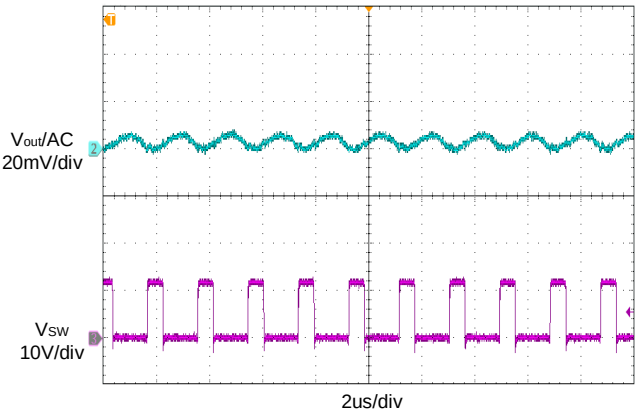


Figure 13. Output Voltage Ripple(I_{OUT}=2A)

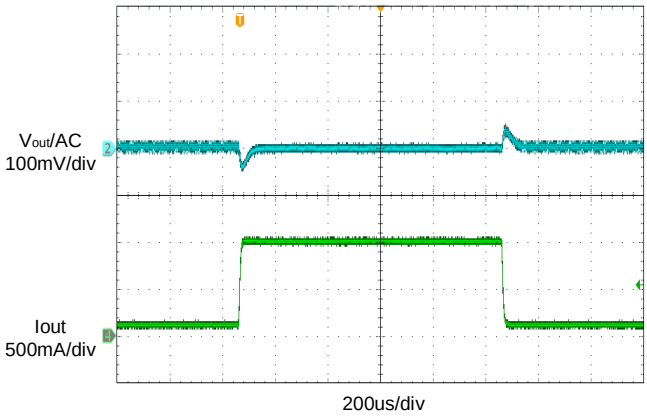


Figure 14. Transient Response(0.1 to 1A)

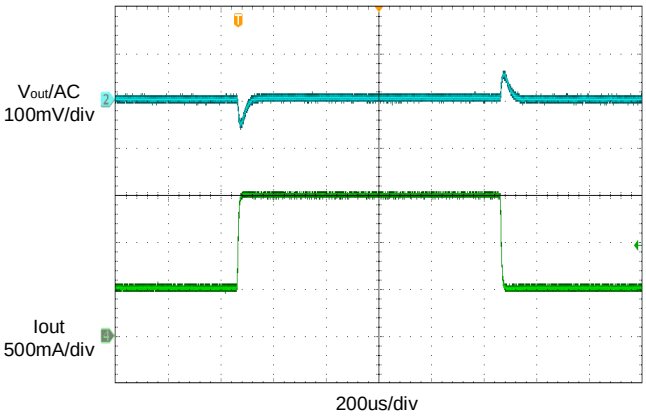


Figure 15. Transient Response(0.5 to 1.5A)

Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 5V, L = 15uH, T_A = 25°C, unless otherwise noted.

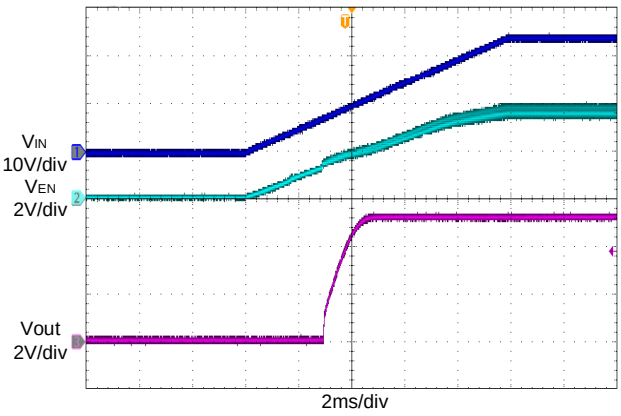


Figure 16. VIN Start-Up without Load

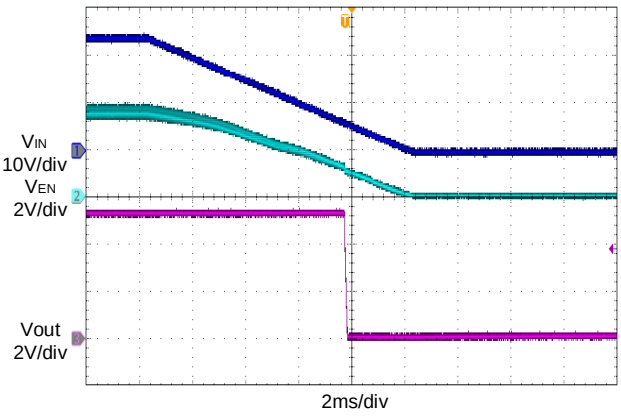


Figure 17. VIN Shut-Down without Load

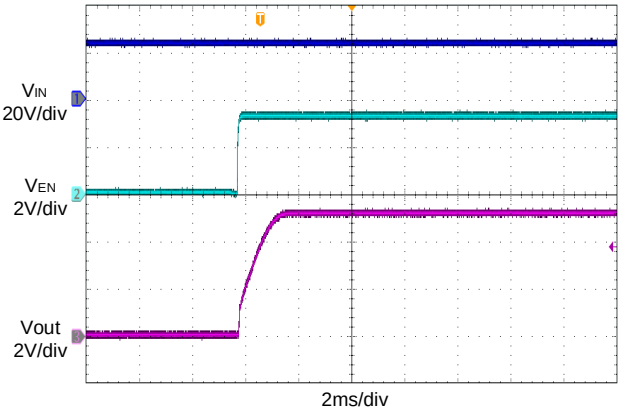


Figure 18. EN Start-Up with Load

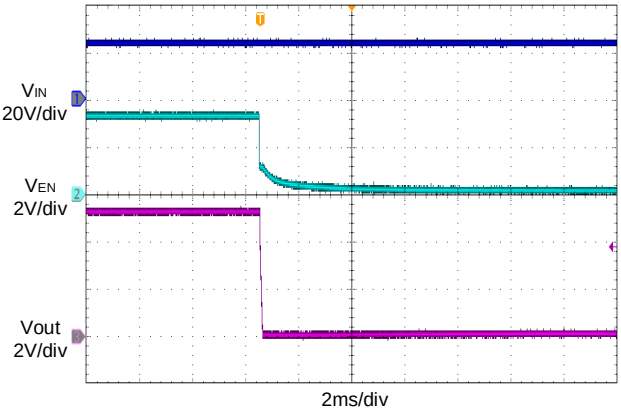


Figure 19. EN Shut-Down with Load

8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues.

1) Place the input/output capacitor and inductor should be placed as close to IC.
2) Keep the power traces as short as possible.
3) The low side of the input and output capacitor must be connected properly to the power GND avoid a GND potential shift.
4) Place the external feedback resistors next to FB.
5) Keep the switching node SW short and away from the feedback network.

For best results, follow the layout example below.

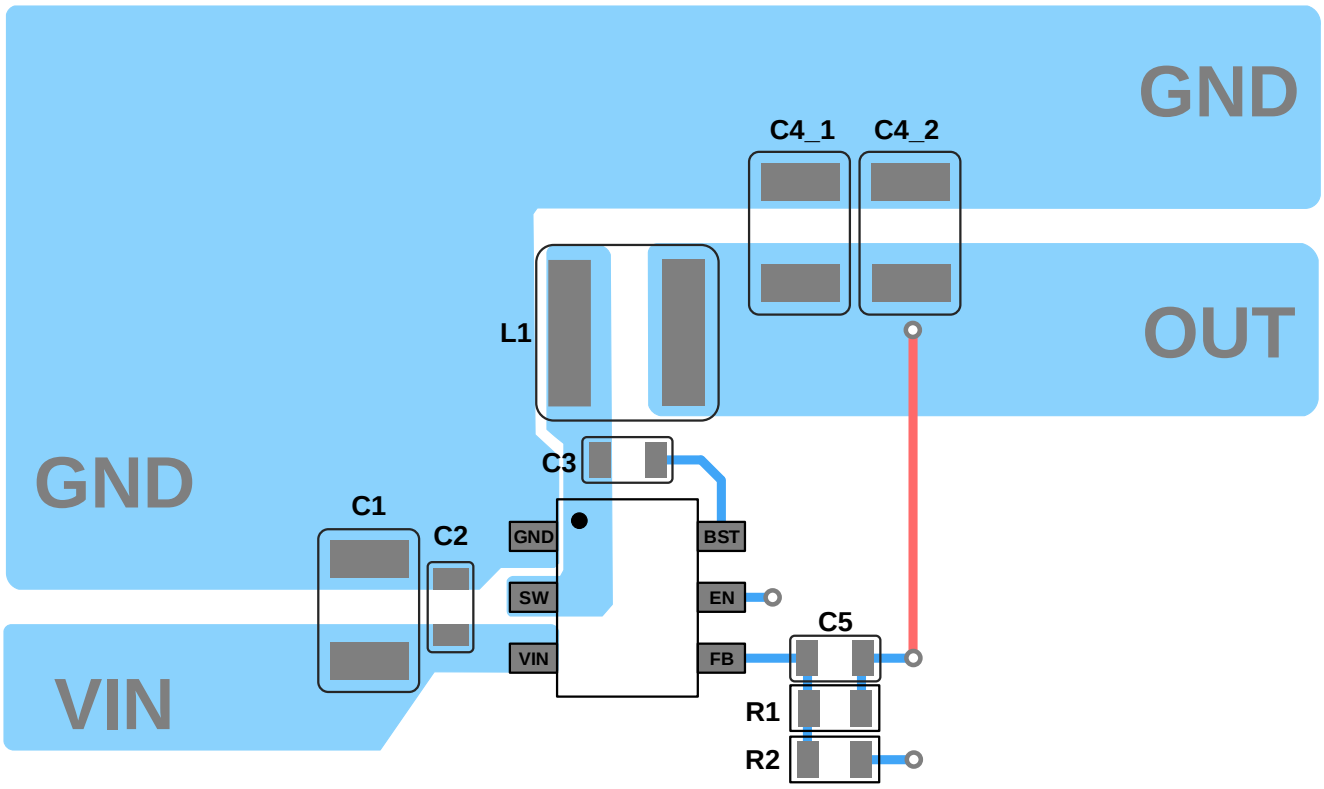
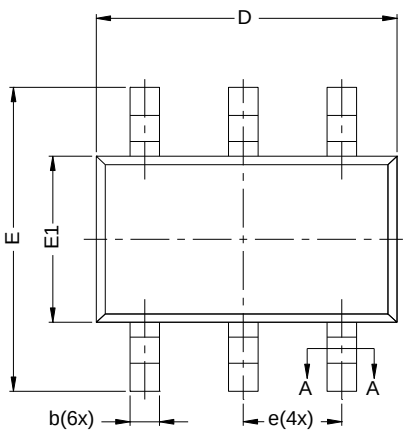


Figure 20. Typical GD30DC1351 Example Layout

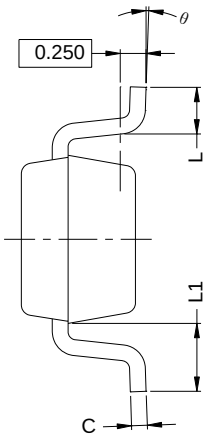
9 Package Information

9.1 Outline Dimensions

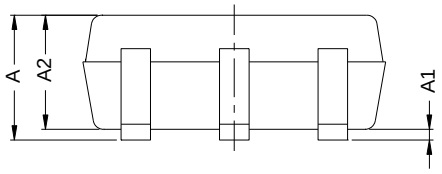
SOT23-6 Package Outline



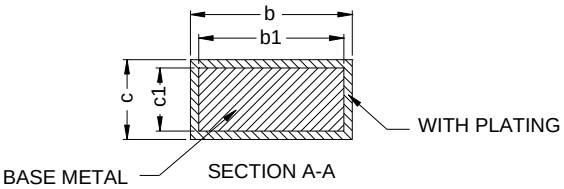
TOP VIEW



SIDE VIEW



FRONT VIEW



SECTION A-A

NOTES:

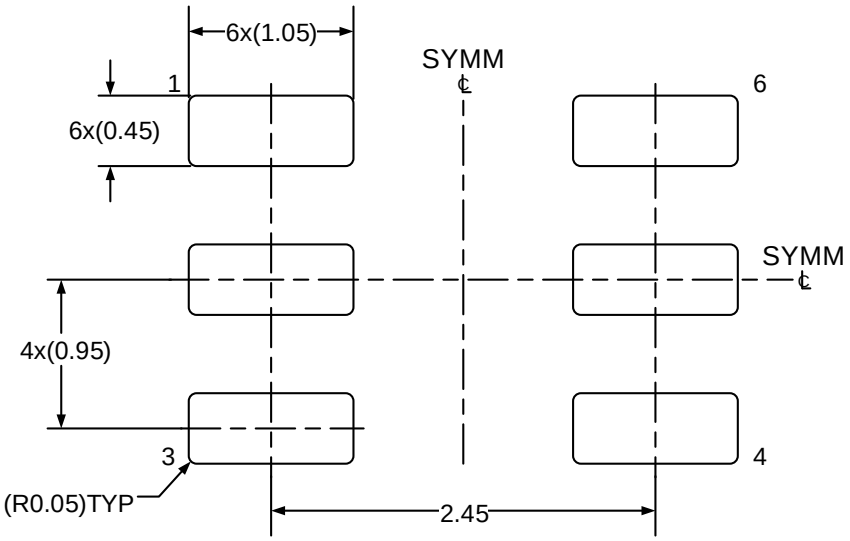
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 4 *SOT23-6 dimensions(mm)*.

Table 4. SOT23-6 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.25
A1	0.04		0.10
A2	1.00	1.10	1.20
b	0.38		0.46
b1	0.37	0.40	0.43
c	0.13		0.17
c1	0.12	0.13	0.14
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.60
L1	0.60 REF		
θ	0°		8°

9.2 Recommended Land Pattern

SOT23-6 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1354SSTR-I	SOT23-6	Green	Tape & Reel	3000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2025

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